This listing of claims will replace all prior versions, and listings of the claims in the application:

Listing of Claims

1. (Currently Amended) A switching ~~Switching~~ arrangement for transporting data packets ~~(a, b, c, d, e)~~ which comprise a section with data packet destination information and a payload section, said data packets ~~(a, b, c, d, e)~~ heading via one or more input ports ~~(20)~~ of a switching device ~~(15)~~ towards one or more output ports ~~(30)~~, said switching device ~~(15)~~ being able to route said ~~arriving~~ data packets ~~(a, b, c, d, e)~~ according to said data packet destination information, to at least one dedicated of said output ports ~~(30)~~, comprising at each input port ~~(20)~~ an input buffer ~~(11)~~ with at least as many single input queues ~~(12)~~ as said switching arrangement has output ports ~~(30)~~, and an input controller ~~(25)~~ for each input port ~~(20)~~, serving for controlling the order of multiplexing said data packets ~~(a, b, c, d, e)~~ from said input queues ~~(12)~~ of said corresponding input buffer ~~(11)~~ to said switching device ~~(15)~~, comprising a demultiplexer ~~(19)~~ for making for each of said ~~arriving~~ data packets ~~(a, b, c, d, e)~~ an entry into those of said input queues ~~(12),~~ which are identified in said packet destination information of the corresponding data packet ~~(a, b, c, d, e)~~, whereby each said input controller ~~(25)~~ is designed to allow simultaneous transmission of those data packets ~~(a, b, c, d, e)~~ whose entries are located in different of said input queues ~~(12)~~ and whose payload sections have identical content.

2. (Currently Amended) A switching ~~Switching~~ arrangement according to claim 1, characterized in that each said entry comprises at least the payload section of the corresponding data packet ~~(a, b, c, d, e)~~.

3. (Currently Amended) A switching ~~Switching~~ arrangement according to claim 1, characterized in that each said entry comprises a pointer to a memory cell wherein at least the payload section of the corresponding data packet ~~(a, b, c, d, e)~~ is stored, said memory cell preferably being located in a common input buffer ~~(23)~~.

4. (Currently Amended) A switching ~~Switching~~ arrangement according to claim 3, characterized in that for the case said data packet ~~(a, b, c, d, e)~~ being a multicast data packet, the demultiplexer ~~(19)~~ is designed to make several entries in said input queues ~~(12)~~ and only one entry of the payload section thereof in a said memory cell.

5. (Currently Amended) A switching ~~Switching~~ according to claim 1, characterized in that only those data packets ~~(a, b, c, d, e)~~ whose entries are located in different of said input queues ~~(12)~~ and whose payload sections have identical content, and whose entries's locations in the respective input queue ~~(12)~~ have the same ranking, are simultaneously transmittable.

6. (Currently Amended) A switching ~~Switching~~ arrangement according to claim 1, characterized in that only those data packets ~~(a, b, c, d, e)~~ are simultaneously transmittable, whose entries are stored in a said input queue ~~(12)~~ of a

said input buffer (II), whose input port ~~(30)~~ is free to receive said data packets ~~(a, b, c, d, e)~~.

7. (Currently Amended) A switching ~~Switching~~ arrangement according to claim 1, characterized in that the switching device ~~(15)~~ comprises an input router ~~(13)~~ and an output router ~~(14),~~ said switching arrangement further comprising a common output buffer ~~(35)~~ with addresses for the data packets ~~(a, b, c, d, e)~~ and address-managing means ~~(16)~~ for managing the use of said addresses of said common output buffer ~~(35)~~, output-queue-manager ~~(17)~~ for entering order information, about at which addresses said data packets ~~(a, b, c, d, e)~~ are stored in said common output buffer ~~(35)~~, into output queues ~~(18)~~ which are connected to said output router ~~(14).~~

8. (Currently Amended) A switching ~~Switching~~ arrangement according to claim 7, characterized in that the output queues ~~(18)~~ provide in total more queuing places for the order information than the common output buffer ~~(35)~~ has addresses, preferably the difference between the total number of places in the output queues ~~(18)~~ and the total number of addresses in the common output buffer ~~(35)~~ being lower than 50% of the total number of addresses.

9. (Currently Amended) A switching ~~Switching~~ arrangement according to claim 7, characterized in that for the output queues ~~(18)~~ and/or for the common output buffer ~~(35)~~ a backpressure generator is provided for signalizing to the input buffers (I I) that a threshold value of occupied places in one or more of the output queues ~~(18)~~ respectively of occupied addresses in the common output buffer ~~(35)~~ is exceeded.

10. (Currently Amended) A switching ~~Switching~~ arrangement according to claim 7, characterized in that for a multicast data packet ~~(d, e)~~ the order information thereof is enterable in each of the output queues ~~(18)~~ for the output ports ~~(30)~~ this multicast data packet ~~(d, e)~~ is intended to reach and that the address thereof is only releasable by the address manager ~~(16)~~ for another data packet, when all order information of said multicast data packet has been successfully processed by the output router ~~(14).~~

11. (Currently Amended) A switching ~~Switching~~ arrangement according to claim 1, characterized in that for data packets ~~(a, b, c, d, e)~~ with different handling-priorities, for each class of priority and for each output port ~~(30)~~ a separate input queue ~~(12)~~ is provided.

12. (Currently Amended) A switching ~~Switching~~ method for data packets ~~(a, b, c, d, e)~~ heading for one or more output ports (30) of a switching arrangement, comprising the steps of:

[-] sorting said data packets ~~(a, b, c, d, e)~~ at each input port ~~(20)~~ according to the output ports ~~(30)~~ which said data packets ~~(a, b, c, d, e)~~ have as destination according to data packet destination information, into input queues ~~(12)~~ of an input buffer ~~(11)~~ which

comprises at least as many of said input queues (12) as said switching arrangement has output ports (30), by making for each of said data packets (a, b, c, d, e) an entry into those of said input queues (12), which are identified in

said packet destination information of the corresponding data packet (a, b, c, d, e),

[-] multiplexing said data packets from said input queues ~~(12)~~ of their corresponding input buffer ~~(11)~~ to a ~~said~~ switching device ~~(15)~~,

[-] controlling with an input controller ~~(25)~~ for each input port ~~(20),~~ the order of said data packets being multiplexed, whereby simultaneous transmission of those data packets ~~(a, b, c, d, e)~~ is allowed, whose entries are located in different of said input queues ~~(12)~~ and whose payload sections have identical content.

[-] routing said data packets ~~(a, b, c, d, e)~~ according to said data packet destination information, to at least one dedicated of said output ports ~~(30)~~ via said switching device ~~(15)~~.

13. (Currently Amended) A switching ~~Switching~~ method according to claim 12, characterized in as each said entry at least the payload section of the corresponding data packet ~~(a, b, c, d, e)~~ is used.

14. (Currently Amended) A switching ~~Switching~~ method according to claim 12, characterized in that as each said entry a pointer to a memory cell wherein at least the payload section of the corresponding data packet ~~(a, b, c, d, e)~~ is stored, said memory cell preferably being located in a common input buffer ~~(23)~~.

15. (Currently Amended) A switching ~~Switching~~ method according to claim 14, characterized in that for the case

said data packet ~~(a, b, c, d, e)~~ being a multicast data packet ~~(d, e)~~, several entries are made in said input queues ~~(12)~~ and the payload section thereof is stored only once in said memory cell.

16. (Currently Amended) A switching ~~Switching~~ method according to claim 12, characterized in that only those data packets ~~(a, b, c, d, e)~~ whose entries are located in different of said input queues ~~(12)~~ and whose payload sections have identical content and whose ~~entries's~~ entry locations in the respective input queue ~~(12)~~ have the same ranking, are allowed to be simultaneously transmitted.

17. (Currently Amended) A switching ~~Switching~~ method according to one of claim 12, characterized in that only those data packets ~~(a, b, c, d, e)~~ are allowed to be simultaneously transmitted, whose entries are stored in a said input queue ~~(12)~~ of a said input buffer ~~(11)~~ whose input port ~~(30)~~ is free to receive said data packets ~~(a, b, c, d, e)~~.

18. (Currently Amended) A switching ~~Switching~~ method according to claim 12, characterized in that the data packets ~~(a, b, c, d, e)~~ are routed via an input router ~~(13)~~ to a common output buffer ~~(35)~~ with addresses for said data packets ~~(a, b, c, d, e)~~, and order information, about at which addresses said data packets ~~(a, b, c, d, e)~~ are stored in said common output buffer ~~(35),~~ is entered into output queues ~~(18)~~ which are connected to an output router ~~(14)~~ being part of said switching device ~~(15)~~.

19. (Currently Amended) A switching ~~Switching~~ method according to claim 18, characterized in that for the order

information in the output queues ~~(18)~~ in total more queuing places are provided, than the common output buffer ~~(35)~~ has addresses.

20. (Currently Amended) A switching ~~Switching~~ method according to claim 18, characterized in that for a multicast data packet ~~(d, e)~~ the order information thereof is entered in each of the output queues ~~(18)~~ for the output ports ~~(30)~~ which this multicast data packet ~~(d, e)~~ is intended to reach and that the address thereof is only released by the address managing means ~~(16)~~ for another data packet ~~(a, b, c, d, e)~~, when all order information of said multicast data packet ~~(d, e)~~ has been successfully processed by the output router ~~(14)~~.

21. (Currently Amended) A switching ~~Switching~~ method according to claim 18, characterized in that when a threshold value of occupied places in one or more of the output queues ~~(18)~~ respectively of occupied addresses in the common output buffer ~~(35)~~ is exceeded, this is signalized to the input buffers ~~(11)~~.